REMARKS

Claims 1-3, 5-9, 11-15, 17-21 and 23 are pending in the present case. Claims 1, 3, 7, 9, 13, 15, 19, and 21 are amended herein. Applicant respectfully requests reconsideration in view of the above amendments to the present application, and the arguments set forth below. No new matter is added herein.

REJECTIONS UNDER 35 USC § 102

STARK (OR EITRHEIM)

Claims 1-3 and 5 are rejected under 35 USC 102(b) over U.S. Patent Application Publication No. 2002/0017936 A1 by Stark, et al. (hereinafter Stark) or European Patent Application No. 570158A2 by Eitrheim et al. (hereinafter Eitrheim). Claim 1 is amended herein as shown below. Applicants have reviewed the cited references and respectfully assert that Claim 1, as amended herein, and its dependent claims are allowable over Stark or Eitrheim for the following rationale.

As amended herein, independent Claim 1 reads as shown below, with underlining added for emphasis.

> 1. A clock signal duty cycle stabilization circuit, comprising:
> an edge detection circuit <u>having a first delay and</u> configured to receive an external clock signal and generate an output therefrom; and
> a <u>non-overlapping clock generator comprising a feedback path having a second delay, the non-overlapping clock generator</u> coupled to receive a first signal comprising the output from the edge detection circuit and a second signal comprising an output from a conditioning circuit, the <u>non-overlapping clock generator</u> configured to produce an internal clock signal having a rising edge generated with the first signal and a falling edge generated with the second signal wherein the internal clock signal

has a duty cycle that is independent of the duty cycle of the external clock, the non-overlapping clock generator further configured to produce a first sample signal, a second sample signal, a first hold signal, and a second hold signal;

wherein the first delay is equal to or greater than the second delay.

Claims 2-3 and 5 depend upon independent Claim 1. As amended herein, independent Claim 1 recites an edge detection circuit having a first delay, a non-overlapping clock generator comprising a feedback path having a second delay, the non-overlapping clock generator configured to produce a first sample signal, a second sample signal, a first hold signal, and a second hold signal, wherein the first delay is equal to or greater than the second delay. These elements are shared by each of its dependent claims, including Claims 2-3 and 5.

Applicants have reviewed the cited references and respectfully submit that neither Stark nor Eitrheim teaches the above referenced limitations. Specifically, Applicants note that neither reference teaches that the delay of an edge detection circuit must be equal to or greater than the delay of a feedback path of a non-overlapping clock generator, as recited in Claim 1. Therefore, since both Stark and Eitrheim fail to teach at least one element recited in amended Claim 1, Applicants respectfully submit that Claim 1 as amended is not anticipated by Stark or Eitrheim, that Claim 1 overcomes the rejection under 35 U.S.C. § 102(b), and is thus in condition for allowance. Moreover, Applicants respectfully submit that claims 2, 3, and 5 also overcome the rejections under 35 U.S.C. § 102(b) and are in condition for allowance as being dependent on an allowable base claim.

REJECTIONS UNDER 35 USC § 103

STARK (OR EITRHEIM) IN VIEW OF HUYNH

Claims 6-9 and 11-12 are rejected under 35 USC 103(a) over Stark (or Eitrheim) in view of U.S. Patent Application Publication No. 2003/0107432 A1 by Huynh (hereinafter Huynh). Applicants have reviewed the cited reference and respectfully assert that Claims 1 and 7, as amended herein, and their respective dependent claims are allowable over Stark (or Eitrheim) in view of Huynh for the following rationale.

Independent Claim 7 is amended herein after a similar fashion as Claim 1 to recite an edge detection circuit having a first delay, a non-overlapping clock generator comprising a feedback path having a second delay, the non-overlapping clock generator configured to produce a first sample signal, a second sample signal, a first hold signal, and a second hold signal, wherein the first delay is equal to or greater than the second delay, as exemplified for the Examiner's convenience above with reference to Claim 1. Applicants respectfully repeat each and every point asserted above in regards to the Stark and Eitrheim references and respectfully re-assert that Stark or Eitrheim do not teach or suggest the above referenced limitations. Specifically, Applicants note that neither reference teaches that ***the delay of an edge detection circuit must be equal to or greater than the delay of a feedback path of a non-overlapping clock generator***, as recited in Claims 1 and 7. Applicants find nothing in Huynh that cures these defects of Stark or Eitrheim.

As Applicants understand the reference, Huynh teaches a switched capacitor amplifier for a pipestaged analog to digital converter (ADC). Huynh ¶ 20. However, Applicants find nothing in Huynh directed towards ***the delay of an edge detection circuit being equal to or greater than the delay of a feedback path of a non-overlapping clock generator***, as recited in Claims 1 and 7 and their respective dependent claims. Applicants find nothing in Stark which cures this defect of Huynh. For at least this reason, Applicants respectfully assert that Claims 6-9 and 11-12 are not taught or suggested by the combination of Stark and Huynh and in fact, that no motivation exists in either reference to combine them in such a way as to produce this recited element and are thus allowable over the cited references, individually or combined, under 35 USC 103(a).

STARK (OR EITRHEIM) IN VIEW OF HUYNH AND DAVIS

Claims 13-15, 17-21 and 23 are rejected under 35 USC 103(a) over Stark (or Eitrheim) in view of Huynh and U.S. Patent No. 5,394,114 A to Davis (hereinafter Davis). Claim 1 is amended herein as shown above. Applicants have reviewed the cited reference and respectfully assert that Claims 1, 7, 13, and 19, as amended herein, are allowable over Stark for the following rationale.

Independent Claims 13 and 19 are amended herein after a similar fashion as Claim 1 to recite an edge detection circuit having a first delay, a non-overlapping clock generator comprising a feedback path having a second delay, the non-overlapping clock generator configured to produce a first sample signal, a second sample signal, a first hold signal, and a

second hold signal, wherein the first delay is equal to or greater than the second delay, as exemplified for the Examiner's convenience above with reference to Claim 1. Applicants respectfully repeat each and every point asserted above in regards to the Stark and Eitrheim references and respectfully re-assert that Stark or Eitrheim do not teach or suggest the above referenced limitations. Specifically, Applicants note that neither reference teaches that ***the delay of an edge detection circuit must be equal to or greater than the delay of a feedback path of a non-overlapping clock generator***, as recited in Claims 13 and 19. Applicants find nothing in Davis that cures this defect of Stark and respectfully reiterate that nothing in Huynh cures these defects of Stark, even combined with Davis.

Applicants respectfully repeat each and every point asserted above in regards to the Huynh reference and respectfully re-assert that Huynh does not teach or suggest ***the delay of an edge detection circuit being equal to or greater than the delay of a feedback path of a non-overlapping clock generator***, as recited herein. Applicants find nothing in Davis that cures this defect of Huynh and respectfully reiterate that nothing in Stark cures these defects of Huynh, even combined with Davis.

As Applicants understand the reference, Davis teaches a waveform generator derived from a periodic reference signal. Davis, col. 1, ll. 12-14 & col. 2, ll. 44-55. However, Applicants find nothing in Davis directed towards ***the delay of an edge detection circuit being equal to or greater than the delay of a feedback path of a non-overlapping clock generator***, as recited in Claims 13 and 19 and their respective dependent claims. Applicants

find nothing in Stark, Eitrheim or Huynh, individually or combined, which cures this defect of Davis. For at least this reason, Applicants respectfully assert that Claims 13-15, 17-21 and 23 are not taught or suggested by the combination of Stark, Huynh and Davis and in fact, that no motivation exists in either reference to combine them in such a way as to produce this recited element and are thus allowable over the cited references, individually or combined, under 35 USC 103(a).

CONCLUSION

By the rationale stated above, Applicant respectfully asserts that Claims 1-3 and 5 are allowable over the cited reference under 35 USC § 102(b) and that Claims 6-9, 11-15, 17-21 and 23 are allowable over the cited references under 35 USC § 103(a). Accordingly Applicant respectfully requests that the rejection of the respective claims under 35 USC §§ 102(b) and 103(a) be withdrawn and that Claims 1-3, 5-9, 11-15, 17-21 and 23 be allowed.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

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